Amendments To the Specification

Please replace paragraph 0005 with the following amended paragraph:

FIG. 1 shows one possible implementation of a conventional approach to a circuit 10 that is used to regulate the voltage applied to a CPU 26 (i.e., V_{cc}), where the circuit 10 uses an hysteric type of switching regulator. During constant current consumption conditions of CPU 26, the voltage at output node 16 is compared to a reference voltage, which is set to the desired voltage level (e.g., 1V) provided by a reference voltage component such as a Zener diode, bandgap reference, etc. When the voltage at output node 16 is lower than the reference voltage by $-V_H$, a comparator 18 generates a logic high signal, causing metal oxide semiconductor field effect transistor (MOSFET) driver 30 to turn on a switching transistor (Q_{sw}) in the power output stage 14. When Q_{sw} is on, current in the output inductor (L), ramps up. If the voltage at output 16 is greater than the reference voltage by $+V_H$, comparator 18 outputs a logic low signal, causing MOSFET driver 30 to turn off Q_{sw} and turn on a synchronization transistor (Q_{SYNC}). When Q_{SYNC} is on, the current through the output inductor ramps down toward zero amps from a peak value. It should be noted that ~~CC~~ voltage regulator 12 has been simplified for discussion purposes and that inductor current ramping is a well-known phenomen~~a~~, described with the following equations.

$$v(t) = L\frac{di(t)}{dt} \qquad \textbf{Equation 1.}$$

Please replace paragraph 0006 with the following amended paragraph:

According to Equation 1 the inductor ramp up rate is:

$$\frac{di(t)}{dt} = \frac{V_{DC} - V_{CC}}{L}$$ **Equation 2**

where V_{DC} is the system voltage, and the inductor ramp down rate is:

$$\frac{di(t)}{dt} = \frac{V_{CC}}{L}$$ **Equation 3.**

Since the system voltage (e.g., ~~V_{CC}~~V_{DC}) is typically on the order of 8.4-21 volts, and therefore much greater than the processor voltage, there is a much higher voltage across the output inductor during the ramp up mode than during the ramp down mode. As a result, the current ramp up rate through the inductor is substantially faster than that of the ramp down rate. Since the ramp down rate is relatively slow, the voltage surge at the output node 16 is typically greater than the voltage droop associated with the ramp up mode. The voltage surge can be estimated as follows, where V_{ESR} is the initial voltage at node 16 (V_{ESR} is not shown in the figure), and i_L is the current through inductor L.

$$v_{SURGE}(t) = \frac{1}{C}\int (i_L - I_{CPU})dt + V_{ESR}$$ **Equation 4.**

Please replace paragraph 0007 with the following amended paragraph:

Due to the tight space limitations associated with mobile computing platforms, a possible output decoupling that will minimize the space of the decoupling solution can achieved by using a multi-layer ceramic capacitors (MLCCs) 22 connected to the output node 16, where MLCCs 22 ~~have~~ has a small form factor. Though in real application several MLCCs will be used to achieve the needed minimum total capacitance for simplicity Figure 1 shows only one capacitor. The MLCCs 22 ~~have~~ has a relatively small equivalent series resistance (ESR), but unfortunately ~~have~~ has a relatively low capacitance. It can be shown from Equation 4 that by using an MLCCs 22 for output decoupling, V_{ESR} can be quite negligible. Due to the low capacitance, however, the voltage surge for the MLCCs 22 can be significantly larger because C appears in the denominator of Equation 4. FIG. 2 shows the estimated voltage surge for a conventional power output stage in plot 24, where a 200 nH output inductor is used. In the illustrated example, the voltage surge threshold (V_{MAX}) is exceeded due to the relatively slow ramp down rate.

Please replace paragraph 0009 with the following amended paragraph:

The various advantages of the embodiments of the present invention will become apparent to one skilled in the art by reading the following specification and appended claims, and by referencing the following drawings, in which the same reference characters refer to the same parts throughout the specification, and in which:

Please replace paragraph 0020 with the following amended paragraph:

Turning now to FIG. 4A, one approach to a circuit 36 is shown in greater detail. Since the power conversion efficiency of a voltage is critical in maintaining a low total platform power consumption to extend the platform's battery life, the voltage regulator of controller circuit 12 is designed to maximize its power-conversion efficiency to minimize power loss. Notebook computers use switching voltage regulators instead of linear-mode voltage regulators due to the much higher power-conversion efficiency. Generally, circuit 36 includes a controller circuit 12, which has a voltage comparator 18 that contains some amount of hysteresis +/-V_H. The circuit ~~to~~ 36 also includes a power output stage 38 having an output node 46. Q_{SW} of the output stage 38, when in the on-state, is used to apply V_{DC} input power to the inductor L. This action causes the current in the inductor to ramp up, providing current to the CPU and the output capacitor 22. Once the output voltage V_{CC} is high enough (e.g., slightly higher than that of the bandgap reference 28), the voltage comparator 18 outputs a logically low condition. In response to the low condition, a Mosfet Driver 30 drives the gate of Q_{SW} low, turning it off. After a small delay such as approximately 10-50 nanoseconds, which is enough time for Q_{SW} to go from an on-state to an off-state, the Mosfet Driver 30 drives the gate of Q_{SYNC} high, turning it on. When Q_{SYNC} is on, the inductor's current ramps down because its voltage is now reversed. As a result, the charge on the output capacitor 22 is depleted/discharged by the CPU 40. After a certain amount of time, when the potential on the capacitor 22 is discharged lower than that of the bandgap reference 28, the voltage comparator 18 changes its polarity from a low to a high condition. In response to the high condition, the Mosfet Driver 30 turns off Q_{SYNC} and sequentially turns on Q_{SW} . This process repeats continuously at a certain frequency. This frequency is referred to as the operating frequency of the voltage regulator. Simply put, the CC 12 switches the power output stage 38 into a current ramp down mode based on detection of a voltage surge at the

output node 46. Similarly, the CC 12 switches the power output stage 38 into a current ramp up mode based on detection of a voltage droop at the output node 46.

Please replace paragraph 0025 with the following amended paragraph:

In order to provide drive strength, the surge notification output 56 of the CPU 40 is coupled to the surge transistor 60 through a buffer 62. In addition, the second terminal of the output inductor 52 is coupled to the output node 46 through a sensing resistor (Rs). The OST 64 receives a level signal from the CPU 40 and converts the level signal into a pulse signal with controlled pulse width duration based on a ramp down current measurement obtained from the sensing resistor prior to surge notification signal activation. SURGE is a one-shoot signal, labeled as such in fig.s 4A and 4B, that is generated by the OST block. It is logically-high long enough to reduce the surge voltage effect. The OST 64 can be implemented by using digital or analog design techniques using commercially available hardware or through integrated circuit design techniques.